

### **Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

### **Listing of Claims:**

1. (currently amended) Method of operating a driving circuit for a display system, wherein the sequence of writing and/or reading video data into and/or from a memory is controlled by means of an address sequencer, each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line, ~~characterized in that the method comprising:~~

~~switching means operate~~ operating the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers from a block of line pointers in address table register means with the output of pixel counting means, and in a second mode wherein a block of line pointers from a full table of line pointers in said memory is downloaded into said address table register means.

2. (currently amended) Driving circuit for a display system comprising:

a memory for video data to be displayed and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory, characterized in that the memory contains a full table of line pointers, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for a block of line pointers from said table of line pointers;

means for successively updating the address table register means with subsequent blocks of line pointers, ~~and;~~

pixel counting means, the output of which in combination with the consecutive line pointers from the address table register means determines the addresses for said video data; and

switching means, by which alternately memory addresses for video data are generated in a first mode in the address sequencer, and in a second mode the address table register is updated with a next block of line pointers.

3. (canceled)

4. (previously presented) Driving circuit as claimed in claim 2, characterized in that the memory comprises a full table of line pointers for different sequences of video data to be displayed.

5. (currently amended) Apparatus for displaying images comprising a display system and a driving circuit according to ~~any one of the~~ claim 2.

6. (canceled)

7. (currently amended) A computer readable medium that stores a computer ~~Computer~~ program capable of running on signal processing means in a driving circuit for a display system according to ~~any one of the~~ claim 2 ~~or in the apparatus according to claim 5.~~

8. (canceled)

9. (new) Driving circuit for a display system comprising:

a memory for video data to be displayed and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory, characterized in that the memory contains a full table of line pointers for different sequences of video data to be displayed, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for a block of line pointers from said table of line pointers;

means for successively updating the address table register means with subsequent blocks of line pointers; and

pixel counting means, the output of which in combination with the consecutive line pointers from the address table register means determines the addresses for said video data.

10. (new) A computer readable medium that stores a computer program capable of running on signal processing means in an apparatus for displaying images according to claim 5.